# Laboratory 1

(Due date: **002/003**: September 25th, **004**: September 26th, **005**: September 27th)

## OBJECTIVES

- ✓ Introduce VHDL Coding for FPGAs.
- ✓ Learn to write testbenches in VHDL.
- ✓ Learn the Xilinx FPGA Design Flow with the Vivado HL: Synthesis, Simulation, and Bitstream Generation.
- ✓ Learn how to assign FPGA I/O pins and download the bitstream on the Nexys™-4 DDR Artix-7 FPGA Board.

## VHDL CODING

- ✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

## NEXYS™-4 DDR ARTIX-7 FPGA BOARD SETUP

- The Nexys-4 DDR Board can receive power from the Digilent USB-JTAG Port (J6). Connect your Board to a computer via the USB cable. If it does not turn on, connect the power supply of the Board.
- Nexys-4 DDR documentation: Available in class website.

## FIRST ACTIVITY (100/100)

- **PROBLEM**: A lock is opened (f='1') only for three combinations of switches: `1001, 0111, 0001`, where '1' represents the ON position of a switch and '0' the OFF position.

  - ✓ Complete the truth table for this circuit:

| a | b | c | d | f |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | |
| 0 | 0 | 0 | 1 | |
| 0 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | |
| 0 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 0 | |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 0 | |
| 1 | 0 | 0 | 1 | |
| 1 | 0 | 1 | 0 | |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 0 | 0 | |
| 1 | 1 | 0 | 1 | |
| 1 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 1 | |

  - ✓ Simplify the Boolean expression:

    $f =$

- **VIVADO DESIGN FLOW FOR FPGAs (follow this order strictly)**:
  - ✓ Create a new Vivado Project. Select the **XC7A100T-1CSG324 Artix-7 FPGA** device.
  - ✓ Write the VHDL code that implements the simplified Boolean expression. Synthesize your circuit (Run Synthesis).
  - ✓ Write the VHDL testbench to test every possible combination of the inputs.
  - ✓ Perform Functional Simulation (Run Simulation → Run Behavioral Simulation). **Demonstrate this to your TA.**
  - ✓ I/O Assignment: Create the XDC file.
    **Nexys-4 DDR Board**: Use `SW0, SW1, SW2, SW3` as inputs, and `LED0` as the output. All I/Os are active high.
  - ✓ Implement your design (Run Implementation).
  - ✓ Do Timing Simulation (Run Simulation → Run Post-Implementation Timing Simulation). **Demonstrate this to your TA.**
  - ✓ Generate the bitstream file (Generate Bitstream).
  - ✓ Download the bitstream on the FPGA (Open Hardware Manager) and test. **Demonstrate this to your TA.**

- Submit (as a .zip file) the generated files: VHDL code, VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

**TA signature:** _____ **Date:** _____


Instructor: Daniel Llamocca
TAs: Jing Wu, Michael Lohrer, Chandana Munireddy